What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

a first well region formed on a surface region of said semiconductor substrate, said first well region having therein at least one MOS transistor and having at least one NMOS finger thereon;

a second well region formed on a surface region of said semiconductor substrate; and

a well ring formed on a surface region of said semiconductor substrate and disposed between said first well region and said second well region, said well ring configured such that said first well region is separated from said second well region other than through a resistance of the semiconductor substrate.

2. The semiconductor device as recited in claim 1, wherein the NMOS finger provides that a resistor is disposed between a gate and VSS.

3. The semiconductor device as recited in claim 2, wherein the gate is configured to act as a high-pass filter.

4. The semiconductor device as recited in claim 1, wherein the well ring is connected to VDD.

5. The semiconductor device as recited in claim 1, wherein the NMOS finger provides that a resistor is disposed between a gate and VSS, wherein the gate is configured to act as a high-pass filter, and wherein the well ring is connected to VDD.

6. The semiconductor device as recited in claim 1, further comprising a diffusion ring which is disposed between the well ring and the first well region.

7. The semiconductor device as recited in claim 6, wherein the diffusion ring is connected to a pMOSFET which is configured to function as a trigger node.

8. The semiconductor device as recited in claim 6, wherein the well ring surrounds the diffusion ring.

9. The semiconductor device as recited in claim 8, wherein the diffusion ring is connected to VSS.

10. The semiconductor device as recited in claim 1, further comprising a diffusion ring which is disposed between the well ring and the first well region, wherein the diffusion ring is connected to a pMOSFET which is configured to function as a trigger node, wherein the well ring surrounds the diffusion ring.

11. The semiconductor device as recited in claim 10, wherein the diffusion ring is connected to VSS.

12. The semiconductor device as recited in claim 1, wherein the NMOS finger comprises a pMOSFE.T having its drain tied to an I/O pad, its source connected to the diffusion ring, and its gate is connected to VDDIO.

13. A semiconductor device comprising:

a semiconductor substrate;

a first well region formed on a surface region of said semiconductor substrate, said first well region having therein at least one MOS transistor and having at least one NMOS finger thereon, wherein the NMOS finger provides that a resistor is disposed between a gate and VSS; and

a second well region formed on a surface region of said semiconductor substrate.

14. The semiconductor device as recited in claim 13, wherein the gate is configured to act as a high-pass filter.

15. The semiconductor device as recited in claim 13, wherein the NMOS finger provides that a resistor is disposed between a gate and VSS, wherein the gate is configured to act as a high-pass filte, and wherein the well ring is connected to VDD.

16. The semiconductor device as recited in claim 13, further comprising a well ring and a diffusion ring which is disposed between the well ring and the first well region.

17. The semiconductor device as recited in claim 16, wherein the diffusion ring is connected to a pMOSFET which is configured to function as a trigger node.

18. The semiconductor device as recited in claim 16, wherein the well ring surrounds the diffusion ring.

19. The semiconductor device as recited in claim 18, wherein the diffusion ring is connected to VSS.

20. The semiconductor device as recited in claim 13, wherein the NMOS finger comprises a pMOSFET having its drain tied to an I/O pad, its source connected to the diffusion ring, and its gate is connected to VDDIO.